In the claims

Kindly cancel claims 20-21 as follows, without prejudice.

1. (Original) A light-sensing pixel, having a p type doped region, in a CMOS image sensor, comprising:

a first doped charge collecting region buried within the p type doped region and configured to operate as a depleted potential well;

a first n+ type doped plug extending from near the surface of the image sensor to the first charge collecting region;

a second doped charge collecting region buried within the p type doped region, the second charge collecting region vertically separated from the first charge collecting region by the p type doped region and configured to operate as a depleted potential well; and

a second n+ type doped plug extending from near the surface of the image sensor to the second charge collecting region.

2. (Original) The pixel of claim 1, the first and second charge collecting regions further comprising:

a first extension with n+ type doping coupled to and between the first charge collecting region and the first plug, and having a different doping concentration than the first charge collecting region; and

a second extension with n+ type doping coupled to and between the second charge collecting region and the second plug, and having a different doping concentration than the second charge collecting region.

3. (Original) The pixel of claim 2 wherein the first and second extensions are configured to operate not fully depleted of mobile charge.

4. (Original) The pixel of claim 1 wherein the first n+ type doped plug contacts the first charge collecting region in its center.

5. (Original) A light-sensing pixel, having a p type doped region, in a CMOS image sensor, comprising:

a first doped charge collecting region buried within the p type doped region and configured to operate as a depleted potential well;

a first vertical trench transistor extending from near the surface of the image sensor to the first charge collecting region;

a first n+ type doped region located at the surface of the image sensor and coupled to the first vertical trench transistor;

a second doped charge collecting region buried within the p type doped region, the second charge collecting region vertically separated from the first charge collecting region by the p type doped region and configured to operate as a depleted potential well;

a second vertical trench transistor extending from near the surface of the image sensor to the second charge collecting region; and

a second n+ type doped region located at the surface of the image sensor and coupled to the second vertical trench transistor.

6. (Original) The pixel of claim 5, the first and second charge collecting regions further comprising:

a first extension with n+ type doping coupled to and between the first charge collecting region and the first vertical trench transistor, and having a different doping concentration than the first charge collecting region; and

a second extension with n+ type doping coupled to and between the second charge collecting region and the second vertical trench transistor, and

having a different doping concentration than the second charge collecting region.

7. (Original) The pixel of claim 6 wherein the first and second extensions are configured to operate not fully depleted of mobile charge.

8. (Original) The pixel of claim 5 wherein the first vertical trench transistor contacts the first charge collecting region in its center.

9. (Original) A light-sensing pixel, having a p type doped region, in a CMOS image sensor, comprising:

a first n+ type doped plug extending from near the surface of the image sensor into the p type doped region;

a first charge collecting region configured to operate as a depleted potential well and buried within the p type doped region, having a first end and a second end and coupled to the first plug at the first end, and having a first vertical slit with a width at the second end, the first vertical slit narrowing towards the first end;

a second n+ type doped plug extending from near the surface of the image sensor into the p type doped region; and

a second charge collecting region configured to operate as a depleted potential well and buried within the p type doped region, having a first end and a second end and coupled to the first plug at the first end, the second charge collecting region vertically separated from the first charge collecting region by the p type doped region, and having a second vertical slit with a width at the second end, the vertical slit narrowing towards the first end.

10. (Original) The pixel of claim 9, wherein the first charge collecting region has a vertical height that is greater than the width of the first vertical slit, and the second charge collecting region has a vertical height that is greater than the width of the second vertical slit.

11. (Original) The pixel of claim 9, the first and second charge collecting regions further comprising:

a first extension with n+ type doping coupled to and between the first charge collecting region and the first plug, and having a different doping concentration than the first charge collecting region; and

a second extension with n+ type doping coupled to and between the second charge collecting region and the second plug, and having a different doping concentration than the second charge collecting region.

12. (Original) The pixel of claim 11 wherein the first extension is coupled to the first end of the first charge collecting region and the second extension is coupled to the first end of the second charge collecting region.

13. (Original) The pixel of claim 11 wherein the first and second extensions are configured to operate not fully depleted of mobile charge.

14. (Original) The pixel of claim 9 wherein the first n+ type doped plug contacts the first charge collecting region in its center.

15. (Original) A light-sensing pixel, having a p type doped region, in a CMOS image sensor, comprising:

a first vertical trench transistor extending from near the surface of the image sensor into the p type doped region;

a first doped charge collecting region buried within the p type doped region and configured to operate as a depleted potential well, having a first end and a second end and coupled to the first vertical trench transistor at the first end, and having a first vertical slit with a width at the second end, the first vertical slit narrowing towards the first end;

a first n+ type doped region located at the surface of the image sensor and coupled to the first vertical trench transistor;

a second vertical trench transistor extending from near the surface of the image sensor into the p type doped region;

a second doped charge collecting region buried within the p type doped region, the second charge collecting region vertically separated from the first charge collecting region by the p type doped region and configured to operate as a depleted potential well, having a first end and a second end and coupled to the second vertical trench transistor at the first end, and having a first vertical slit with a width at the second end, the first vertical slit narrowing towards the first end; and

a second n+ type doped region located at the surface of the image sensor and coupled to the second vertical trench transistor.

16. (Original) The pixel of claim 15, the first and second charge collecting regions further comprising:

a first extension with n+ type doping coupled to and between the first charge collecting region and the first vertical trench transistor, and having a different doping concentration than the first charge collecting region; and

a second extension with n+ type doping coupled to and between the second charge collecting region and the second vertical trench transistor, and having a different doping concentration than the second charge collecting region.

17. (Original) The pixel of claim 16 wherein the first and second extensions are configured to operate not fully depleted of mobile charge.

18. (Original) The pixel of claim 16 wherein the first extension is coupled to the first end of the first charge collecting region and the second extension is coupled to the first end of the second charge collecting region.

19. (Original) The pixel of claim 15 wherein the first vertical trench transistor contacts the first charge collecting region in its center.

20. (Canceled)

21. (Canceled)